WHAT IS CLAIMED IS:

1. A SDH test apparatus for substituting a part of payload of received SDH data with a desired data and transmitting, comprising:

a Rx SOH processor for performing frame detection of said received SDH data;

a Rx AU processor for extracting AU data composed of AU pointer of data processed by said Rx SOH processor and payload, and detecting an information leading head position designated by said AU pointer;

a Tx AU processor for generating AU data wherein a part of payload of AU data extracted by said Rx AU processor is substituted with a desired data;

a Tx SOH processor for generating a new SDH data with AU data generated by said Tx AU processor and data from said Rx SOH processor and transmitting;

a FIFO memory installed between said Rx AU processor and said Tx AU processor, for storing sequentially payload of AU data extracted by said Rx AU processor and outputting to said Tx AU processor in the order of memorization; and

an AU pointer processor for outputting an AU pointer adjusting the number of data in said FIFO memory, allowing said Tx AU processor to read in payload of AU data, after a time lag ($\Delta T2 + \Delta T4$) of information leading head position of payload generated by the processing of AU data by said Rx AU processor

and said Tx AU processor, by extracting the number of data in said FIFO memory,

wherein said Tx AU processor is composed to read out the payload of AU data from said FIFO memory, generate AU data and output to said Tx SOH processor so that said information leading position is at the position designated by the AU pointer value output from said AU pointer processor.

2. A SDH test apparatus according to claim 1 further comprising:

a Rx TU processor for extracting TU data by from data processed by said Rx AU processor;

a second FIFO memory for storing successively the TU data extracted by said Rx TU processor;

a Tx TU processor for performing transmission TU processing for TU data output from said second FIFO memory in the order of memorization; and

a TU pointer processor composed to decide the TU pointer anticipating the information leading head position shifting due to the processing time of TU data by the Rx TU processor and the Tx TU processor, the delay time to maintain said second FIFO memory data storage state stable.

3. A SDH test method for substituting a part of payload of received SDH data with a desired data and transmitting, comprising the steps of:

Rx SOH processing including frame detection of

said received SDH data;

Rx AU processing including extraction of AU data composed of AU pointer of data processed by said Rx SOH processing and payload, and detection of the information leading head position designated by said AU pointer;

Tx AU processing including generation of AU data wherein a part of payload of AU data extracted by said Rx AU processing is substituted with a desired data;

Tx SOH processing including generation of a new SDH data with AU data generated by said Tx AU processing and data by said Rx SOH processing and transmission thereof;

storing sequentially AU data extracted by said Rx AU processing between said Rx AU processing and said Tx AU processing in a FIFO memory and transmitting to said Tx AU processing in the order of memorization; and

AU pointer processing for outputting an AU pointer adjusting the number of data in said FIFO memory, allowing said Tx AU processing to read in payload of AU data, after a time lag ($\Delta T2 + \Delta T4$) of information leading head position of payload generated by the processing of AU data by said Rx AU processing and said Tx AU processing, by extracting the number of data in said FIFO memory,

wherein said Tx AU processing is composed to read out the payload of AU data from said FIFO memory,

generate AU data and output to said Tx AU processing so that said information leading position is at the position designated by the AU pointer value output from said AU pointer processing.

4. A SDH test method according to claim 3, further comprising the steps of:

Rx TU processing for extracting TU data by from data processed by said Rx AU processing;

storing successively the TU data extracted by said Rx TU processing in a second FIFO memory;

Tx TU processing for performing Tx TU processing for TU data output from said second FIFO memory in the order of memorization; and

TU pointer processing to decide the TU pointer anticipating the information leading head position shifting due to the processing time of TU data by the Rx TU processing and the Tx TU processing, the delay time to maintain said second FIFO memory data storage state stable.